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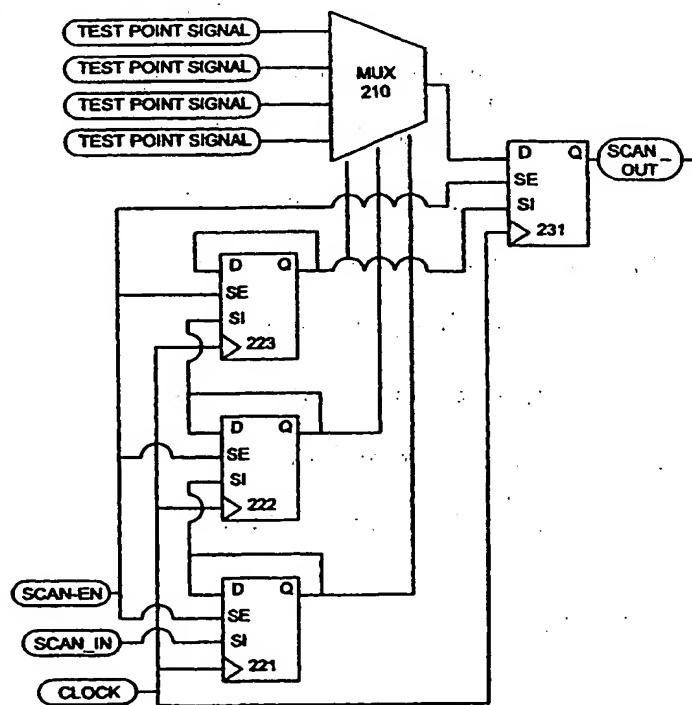
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(54) Title: A SCAN TEST POINT OBSERVATION SYSTEM AND METHOD

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and method collects scan test information from scan test points that would otherwise be difficult to access and provides them at point on a scan chain (e.g. an output of a scan test observation point) that is efficiently observable by an ATPG tool.

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A SCAN TEST POINT OBSERVATION SYSTEM AND METHOD

FIELD OF THE INVENTION

5 The present invention relates to the field of electrical integrated circuit testing. More particularly, the present invention relates to a scan test observation system and method to enhance test observability in integrated circuits utilizing scan test methodologies.

10 BACKGROUND OF THE INVENTION

Electronic systems and circuits have made a significant contribution towards the advancement of modern society and are utilized in a number of applications to achieve advantageous results. Numerous electronic technologies such as digital computers, calculators, audio devices, video equipment, and telephone systems have facilitated increased productivity and reduced costs in analyzing and communicating data, ideas and trends in most areas of business, science, education and entertainment. Frequently, electronic systems designed to provide these results comprise a variety of components or devices including microelectronic integrated circuits. Usually the components or devices of an electronic system are required to operate properly in order for the desired results to be realized. An efficient and

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reliable integrated circuit (IC) testing system and method is very important for assuring an IC operates properly.

- The complexity of commonly used integrated circuits included in
- 5 system-on-chip (SOC) designs has advanced dramatically and built in self test (BIST) diagnostics capability is essential for effective circuit testing, debugging, and maintenance. Modern BIST techniques typically include the insertion of a scan test architecture in an IC to provide controllability and observability of IC components. Typically, scan test architectures include scan test
- 10 components or devices (e.g., scan test cells) that interact with functional logic utilized to perform non-test or normal operations of the IC. Scan testing of complex electronic systems and circuits often requires analysis of measurements from test points (e.g., appropriately selected circuit nodes at the outputs or inputs of functional logic) after the application of test vectors
- 15 to stimulate certain aspects of a circuit (e.g., a functional logic component). For example, microelectronic IC chips typically have numerous signal transmission path connections to external devices and connections between internal functional logic components. These signal transmission path connections are often appropriate circuit nodes for testing activities such as
- 20 fault isolation and detection.

Boundary scan testing is a very common method of scan testing included in typical BIST schemes. International Electrical and Electronic

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Engineering (IEEE) Standard 1149.1 (also referred to as Joint Task Action Group (JTAG)) boundary scan compliant architecture is one of the most prevalent boundary scan schemes. The IEEE 1149.1 boundary scan architecture is primarily utilized to detect and isolate interconnect faults 5 between components. A typical JTAG IEEE 1149.1 boundary scan compliant chip includes a boundary scan test cell or register at input/output (I/O) pins of a chip. Usually a JTAG scan test operation includes placing a known value or test vector on an output buffer of one device and observing the input buffer of another interconnected device to determine if they are electrically 10 connected. However, boundary scan testing is somewhat limited in its ability to provide control and observability of internal connections and devices or components of an IC.

As a general proposition, it is desirable to have significant internal scan 15 test coverage of numerous scan test points. Usually the greater the test coverage the greater the capacity of a scan test system and method to detect faults. Having both internal and boundary scan capability is often referred to as full scan testing. At this time there is no dominant standard with respect to full scan testing architectures. However, most full scan testing techniques 20 rely on scan test cells included in the IC. Typically, the scan test cells are designed to scan or shift scan test information (e.g., test vectors) to appropriate locations in a circuit and capture scan test information from scan test points. For example, in one typical scan test process a particular logical value is

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shifted via scan test cells to the input of a functional component, the functional component performs a normal operation based upon the shifted scan test information, a scan test cell captures the output of the functional component and the captured information is shifted off the chip via scan test cells. Usually the scan test cells are incorporated in the IC during the design. However, typical automated design processes do not adequately accommodate and incorporate sufficient scan test devices (e.g., scan test cells coupled to internal scan test points) to achieve desirable full scan testing coverage levels.

10 Scan test coverage and observability is often limited by difficulties encountered in the actual incorporation of scan test architecture components during IC manufacturing processes. Large portions of a design are often considered untestable as a practical matter primarily because faults in a section of the logic cannot be clearly observed by typical automated test

15 pattern generation (ATPG) tools. Most ATPG tools are capable of identifying appropriate observation points necessary to enhance the maximum fault coverage. However, this information is not typically available until the design has progressed through place and route (P&R) manufacturing processes. Not having the information identifying appropriate observation

20 points until after the place and route process makes it very difficult to implement large logic changes that are often required to accommodate the addition of the appropriate observation points. ATPG tools typically offer significant scan testing advantages (e.g., automation, cost efficiencies, etc.) and

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even though it is difficult, it is desirable to increase the observability of some sections of logic to aid an ATPG tool achieve desirable targeted fault coverage.

Traditional techniques directed to increasing the observability of some sections of logic before generating test patterns by an ATPG tool usually require an extensive knowledge of both the circuit and the algorithms used by an ATPG tool to determine appropriate fault detection. Typically designers do not have an extensive knowledge of both the circuit and the algorithms used by an ATPG tool to determine appropriate fault detection and often one or the other or both of these factors are unknown or unclear to the designer. Some conventional approaches to alleviate test point coverage problems include multiplexing internal logic signals to primary input/output (I/O) pads of the device. However, this conventional approach or solution to alleviating test point coverage problems results in various drawbacks. For example, the conventional solution often adds excessive delays to critical timing paths during normal (non-test) operations. Conventional solutions typically require extensive post layout modifications to the physical design of an IC and making these modifications after layout results in many of the observations points being unreachable or inaccessible as a practical matter by typical ATPG tools.

What is required is system and method that facilitates desirable scan testing of internal components with minimal impacts to normal operations

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and manufacturing processes. The system and method should support efficient scan testing of integrated circuit components with an ATPG tool while providing effective observation of scan test points. The electronic system and method should accommodate utilization of existing testing scan architectures and minimization of adverse redesign impacts to existing IC designs.

SUMMARY OF THE INVENTION

The present invention is a system and method that facilitates desirable scan testing of internal components with minimal impacts to normal operations and manufacturing processes. The scan test observation system and method of the present invention supports efficient scan testing of integrated circuit components with an ATPG tool while providing effective observation of scan test points. The present invention system and method accommodates utilization of existing testing scan architectures and minimization of adverse redesign impacts to existing IC designs. The present invention enhances test observability in digital circuits and is compatible with scan test methodologies.

One embodiment of the present invention includes a scan test observation point system comprising a multiplexer, a control register and an output register. The multiplexer selectively provides a communication path from a test point signal to the output register. The test point signal is a measurement or logical value captured from a functional component of an IC. The control register is utilized to direct the multiplexer which signal to transmit to the output register. The output register receives the signal transmitted from the multiplexer and transmits it on a scan test chain. In one embodiment of the present invention, the control register and the output register are included in a scan test chain and are utilized to shift scan test

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information during a scan test shift mode. In one embodiment of the present invention, the test point signals are assessable to an ATPG tool via the scan test observation point system.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of one embodiment of a scan test observation point system of the present invention.

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Figure 2 is a block diagram of another embodiment of a scan test observation point system of the present invention.

Figure 3 is a block diagram of a present invention integrated circuit
10 including one embodiment of a scan test observation point system.

Figure 4 is a block diagram of one embodiment of a scan test point system comprising a plurality of multiplexers and output registers.

15 Figure 5 is a flow chart of scan test observation point method, one embodiment of the present invention.

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DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the preferred embodiments of the invention, a scan test point observation system and method, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims.

Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one ordinarily skilled in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the current invention.

One embodiment of the present invention includes a scan test observation point system and method. In one embodiment of the present invention, a scan test observation point system is included in a scan testing chain permitting it to be controlled and observed by normal scan testing methodologies. Scan test observation point system logic devices are included

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in a design at various locations during the initial stages of a manufacturing process as spare logic cells in one embodiment of the present invention.

After requisite test points are identified, test point signals are routed to the scan test observation point system. In one embodiment of the present

5 invention, the scan test observation point system facilitates scan testing operations by an ATPG tool. The scan test observation point system is configured in a manner that is compatible with a scan test architecture familiar to the ATPG tool and easily accessible by the ATPG tool.

10 Figure 1 is a block diagram of scan test observation point system 100, one embodiment of the present invention. Scan test observation point system 100 comprises test signal selection component 110, test signal selection control component 120 and output component 130. Test signal selection component 110 is coupled to test signal selection control component 120 and 15 output component 130. In one embodiment of the present invention, scan test observation point system 100 is included in an IC and efficiently provides observation of test points signals to an ATPG tool with minimal impacts to design processes and minimal design rework.

20 The components of scan test observation point system 100 cooperatively operate to facilitate test point observation operations. Test point signal selection component 110 receives and transmits a scan test signal. In one embodiment of scan test observation point system 100, test signal

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selection component 110 receives a plurality of test point signals including test point signal 131, test point signal 132 and test point signal 133 and selectively transmits one of the test point signals to output component 130.

In one embodiment of the present invention, test point signals 131 through 5 133 are measurements (e.g., logical values) from test points in functional logic (not shown) utilized to perform normal operations of an IC. Test signal selection control component 120 controls the receiving and transmitting of the test point signal by test signal selection component 110. Output component 130 receives the scan test signals from test signal selection 10 component 110 and transmits them on a scan test chain.

In one embodiment of the present invention scan test observation point system 100 is included in a scan test chain. In one embodiment of the present invention, test signal selection control component 120 controls test signal component 110 by directing test signal component 110 to transmit a scan test signal based upon scan test information received by test signal selection control component 120 from a scan test input (e.g., scan input signal 155) on the scan test chain. Scan test observation point system 100 is also utilized to shift scan test information on the scan test chain. Scan test signal 15 120 selection control component 120 receives a scan test input signal (e.g., scan input signal 155) and transmits it to output component 130 which forwards 20 the scan test input signal unchanged downstream on the scan test chain.

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Figure 2 is a block diagram of scan test observation point system 200, one embodiment of the present invention. Scan test observation point system 200 comprises test signal selection multiplexer (MUX) 210, control register 221, control register 222, control register 223 and output register 231.

- 5 Multiplexer 210 is coupled to control register 221, control register 222, control register 223 and output register 231. Multiplexer 210 selectively provides a communication path between one of its inputs to its output. The control register 221, control register 222 and control register 223 are utilized to control receiving and transmitting of the input to multiplexer 210 via the output of
- 10 multiplexer 210 to output register 231. In one example of the present invention, the output of control registers 221 through 223 controls the receiving and transmitting of the input to multiplexer 210 by forwarding a signal to multiplexer 210 that selects which input of multiplexer 210 is transmitted out to output register 231. Output register 231 transmits the
- 15 output of multiplexer 210 or scan test input information shifted in via control registers 221 through 223.

- In one embodiment of the present invention, scan test observation point logic devices (e.g., scan test observation point logic devices comprising scan test observation point system 200) are included in an IC design at various locations as spare logic cells in the initial stages of a manufacturing process. The inputs to a multiplexer of a scan test observation point system (e.g., multiplexer 210) are coupled to static signals (e.g., logic 1 or logic 0) as a default

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setting during the initial stages of the manufacturing. After desirable test points are identified, test point signals from the identified test points are routed to the multiplexer inputs and replace some or all of the static signals.

In one embodiment of the present invention, the test point signals are

- 5 accessible to an ATPG tool via an output register of a scan test observation point system.

In one embodiment of scan test observation point system 200, scan test operations include a shift mode and a capture mode. During the shift mode a scan input signal (scan-in) representing scan test input data is shifted in a serial fashion into a scan test chain that includes scan test observation system 200. The shift mode operations are accomplished by applying the scan_in signal to a scan test input port and asserting a scan enable signal (scan_en). As scan test data is shifted into the scan test chain scan test information is also shifted out of the scan test chain as a scan test output signal (scan_out). In one embodiment of the present invention the scan test architecture including scan test observation point system 200 is synchronous and shifting is controlled by a clock signal (clock).

- 20 In one embodiment of scan test observation point system 200, the capture mode is accomplished by deasserting the scan test enable signal and asserting a clock pulse. The value captured by output register 231 is dependent on the values that are shifted into the control registers 221

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through 223. A specific set of values in the control registers 221 through 223 selects one of the test point input signals coupled to multiplexer 210 for transmission to the output of multiplexer 210. In one embodiment scan test observation point system 200, the output of the control registers 221 through 5 223 are fed back into the respective inputs of control registers 222 through 223. Thus, the values stored in the control registers do not change during a capture cycle. In one embodiment of the present invention, the feed back into the control registers 221 through 223 is a preferred method for debugging despite some undetectable defaults. In one embodiment of the present 10 invention, D inputs of control registers are coupled to another scan test observation point system. In yet another embodiment of the present invention the D inputs of the control registers are coupled to different outputs of the control registers. To observe the captured information, the scan enable signal is reasserted and the captured data is shifted out while new 15 values are shifted into the scan chain.

Figure 3 is a block diagram of integrated circuit 300, one embodiment of the present invention. Integrated circuit 300 comprises functional logic 310 and scan test observation point system 320. Functional logic 310 is coupled to 20 scan test observation point system 320. Functional logic 310 is also coupled to scan enable line 312, clock line 313, scan test point bus 315 and scan output line 314. Scan test observation point system 320 is coupled to scan input line 311, scan enable line 312, clock line 313, scan test point bus 315, scan output

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line 314 and scan output line 321.

- The components of integrated circuit 300 cooperatively function to facilitate scan testing of functional logic 310. Functional logic 310 performs normal operations of the IC. Scan input line 311 provides a communications path for scan input signals (e.g., scan_in). Scan enable line 312 provides a communication path for scan enable signals (e.g., scan_en). Clock line 313 provides a communication path for clock signals (e.g., clock). Scan test point bus 315 provides a communication path for test point signals representing scan test information transmitted from functional logic 310. Scan output line 314 and scan output line 321 provide communication paths for scan output signals (e.g., scan_out). In one embodiment of the present invention scan output line 314 carries signals received by functional logic 310 on scan input line 311 and that are passed through functional logic 310 without changing.
- In one embodiment of the present invention scan output line 321 carries scan output signals that comprise scan output signals from scan output line 314 and for scan test information captured from functional logic 310 and transmitted via scan test point bus 315. Scan test observation point 320 includes scan test observation point system 200 and selectively transmits scan test information received from functional logic 310.

It is appreciated that some embodiments of a scan test observation point system receive numerous scan test point signals. For example, one

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- embodiment of a scan test observation system includes a larger test signal selection multiplexer. Another embodiment of a present invention scan test observation point system includes a plurality of multiplexers and output registers facilitating multiple fault captures during a scan test operation
- 5 capture cycle.

- Figure 4 is a block diagram of scan test point system 400, one embodiment of the present invention comprising a plurality of multiplexers and output registers. Scan test point system 400 comprises multiplexer 411, 10 multiplexer 413, control register 421, control register 422, control register 423 and output register 431 and output register 433. Multiplexer 413 is coupled to control register 421, control register 422, control register 423 and output register 433. Multiplexer 411 is coupled to control register 421, control register 422, control register 423 and output register 431. Control registers 421 is 15 coupled to control register 422 which is coupled to control register 423. Control register 423 coupled to output register 431 which is coupled to output register 433.

- The scan test operations of scan test point system 400 are similar to scan 20 test point system 200, except scan test point system 400 facilitates multiple fault captures during a scan test operation capture cycle. Multiplexer 411 and 413 selectively provide a communication path between one of their respective inputs to their respective outputs. The outputs of control register 421, control

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register 422 and control register 423 are utilized to select which input of multiplexer 411 and 413 are transmitted to output register 431 and 433 respectively. Output register 431 and 433 transmit the output of respective multiplexers 411 and 433 or output register 431 and 433 transmit scan test
5 input information.

Figure 5 is a flow chart of scan test observation point method 500, one embodiment of the present invention. Scan test observation point method 500 facilitates scan testing of functional logic within an IC. In one
10 embodiment of the present invention scan test observation point method 500 is utilized to enhance ATPG tool scan test observation point detection and observation.

In step 510, scan test point signals are received from a functional
15 component comprising a test point. In one embodiment of scan test observation point method 500, a scan test point signal is received during a capture mode of a scan test system and is accomplished by deasserting a scan test enable signal and asserting a clock pulse. In one embodiment of the present invention the scan test point signal is a signal received from an
20 output of a functional logic component included in an IC after the functional logic component performs designated operations. In one embodiment of scan test observation point method 500, the functional logic component performs designated operations based upon scan input information shifted in on the

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scan chain and presented to inputs of the functional component.

In step 520 scan test information is selected for transmission on a scan test chain. In one embodiment of the present invention, a scan test point system (e.g., scan test point system 200) selects which scan test information is transmitted on the scan test chain based upon scan test input information. In one example of step 520, a multiplexer is utilized to provide a communication path from one of its inputs to its output based upon control values sent to the multiplexer from control logic. Control values that determine the selection of information transmitted on the scan test chain are shifted in on the scan chain to the control logic (e.g., control registers 121 through 123). In one embodiment scan test observation point method 500, the selection values are stored and retained during capture operations. For example, the selection values are stored in control registers by looping the output of the control registers back into the respective inputs of the control registers (e.g., 121 through 123).

In step 530 the scan test information is transmitted on a scan test chain. In one example of the present invention, the scan test information comprises test point signals and scan test input information. The test point signals include signals captured from test points in functional logic. Scan test input information includes scan test information that is received and transmitted unchanged. In one embodiment of the present invention scan test

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information from the output of a scan test observation point becomes input scan test information for downstream components of a scan test chain during a scan test shifting mode. In one embodiment of the present invention shifting is performed by asserting a scan enable signal (scan_en) and applying 5 an input scan test data signal (e.g., scan_in) to a scan test input port. As scan test data is shifted into a scan test chain scan test information is also shifted out of the scan test chain as a scan test output signal (scan_out). In one embodiment of the present invention the scan test operations are synchronous and shifting is controlled by a clock signal (clock).

10

Thus, the present invention is a system and method that facilitates desirable scan testing of internal components with minimal impacts to normal operations and manufacturing processes. The system and method of the present invention supports efficient scan testing of integrated circuit 15 components with an ATPG tool while providing effective observation of scan test points. A scan test observation point system and method of the present invention accommodates utilization of existing testing scan architectures and minimization of adverse redesign impacts to existing IC designs.

20

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are

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possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

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CLAIMS

What is claimed is:

5 1 A scan test point observation system included in an integrated circuit comprising:

a test signal selection component adapted to receive and transmit a scan test signal;

10 a test signal selection control component coupled to said test signal selection component, said test signal selection control component adapted to control receiving and transmitting of said test point signal by said test signal selection component; and

15 an output component coupled to said test signal selection component, said output component adapted to receive said scan test signal from said test signal selection component and transmit said test signal on a scan test chain.

2 The scan test point observation system of Claim 1 in which said test signal selection component is further adapted to receive a plurality of test point signals and selectively transmit one of said plurality of test point signals to said output component.

3 The scan test point observation system of Claim 1 wherein said scan test signal is a test point signal comprising measurements of logical values

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from test points in functional logic utilized to perform normal operations of an IC.

- 4 The scan test point observation system of Claim 1 wherein said test signal selection control component is adapted to receive a scan test input signal and transmit said scan test input signal to said output component which is adapted to forward said scan test input signal unchanged downstream on said scan test chain.
- 10 5 A scan test point observation system included in an integrated circuit comprising:
 - a test signal selection multiplexer (MUX) adapted to selectively provide a communication path for a signal at an input of said MUX to an output of said MUX;
 - 15 a control register coupled to said MUX, said control register adapted to control receiving and transmitting of said signal at said input to said MUX via said output of said MUX; and
 - an output register coupled to said MUX, said output register adapted to transmit a signal at said output of said MUX or a signal representing scan test input information shifted in via said control register.
- 6 The scan test point observation system of Claim 5 in which said control register controls said receiving and transmitting of said signal at said input to

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said MUX by forwarding a signal to said MUX that selects which input of said MUX is transmitted out to said output register.

7 The scan test point observation system of Claim 5 wherein said signal at said input to said MUX comprises a test point signal.

8 The scan test point observation system of Claim 5 wherein said signal at said input to said MUX is a test point signal forwarded from functional logic during a scan test capture operation.

10

9 The scan test point observation system of Claim 5 wherein said signal at said input to said MUX is a test point signal that is accessible to an ATPG tool via said output register.

15 10 The scan test point observation system of Claim 5 wherein an output of said control register is fed back into an input of said control registers.

11 The scan test point observation system of Claim 5 wherein a D input of said control register is coupled to another scan test observation point system.

20

12 The scan test point observation system of Claim 5 wherein a D input of said control register is coupled to a different output of said control register.

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13 The scan test point observation system of Claim 5 further comprising functional logic coupled to an input of said MUX, said functional logic adapted to perform normal operations of said IC.

5 14 The scan test point observation system of Claim 13 in which scan test information received from said functional logic is selectively transmitted on said scan chain by said output component.

10 15 The scan test point observation system of Claim 5 further comprising a plurality of multiplexers and output registers facilitating multiple fault captures during a scan test operation capture cycle.

15 16 The scan test point observation system of Claim 15 in which said plurality of multiplexers selectively provide a communication path between one of said plurality of multiplexers respective inputs to said plurality of multiplexers respective outputs and said plurality of output registers transmit an output of respective plurality of multiplexers.

17 The scan test point observation system of Claim 5 wherein said control register is controlled by an ATPG tool.

20 18 A scan test point observation method comprising the steps of:
receiving scan test information from a functional component

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comprising a test point;

selecting said scan test information for transmission on a scan chain;

and

transmitting said scan test information on a scan.

5

19 A scan test point observation method of Claim 18 further comprising the steps of:

deasserting a scan test enable signal; and

asserting a clock pulse.

10

20 A scan test point observation method of Claim 18 in which said scan test point signal is a signal received from an output of a functional logic component included in an IC after said functional logic component performs designated operations.

15

21 A scan test point observation method of Claim 18 in which selecting said scan test information for transmission on a scan chain is based upon scan test input information.

20 22 A scan test point observation method of Claim 18 further comprising the step of shifting in control values that determine selection of information transmitted on said scan test chain.

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- 23 A scan test point observation method of Claim 22 further comprising the step of storing said control values during capture operations.
- 24 A scan test point observation method of Claim 18 further comprising
5 the steps of:
asserting a scan enable signal; and
applying an input scan test data signal to a scan test input port.

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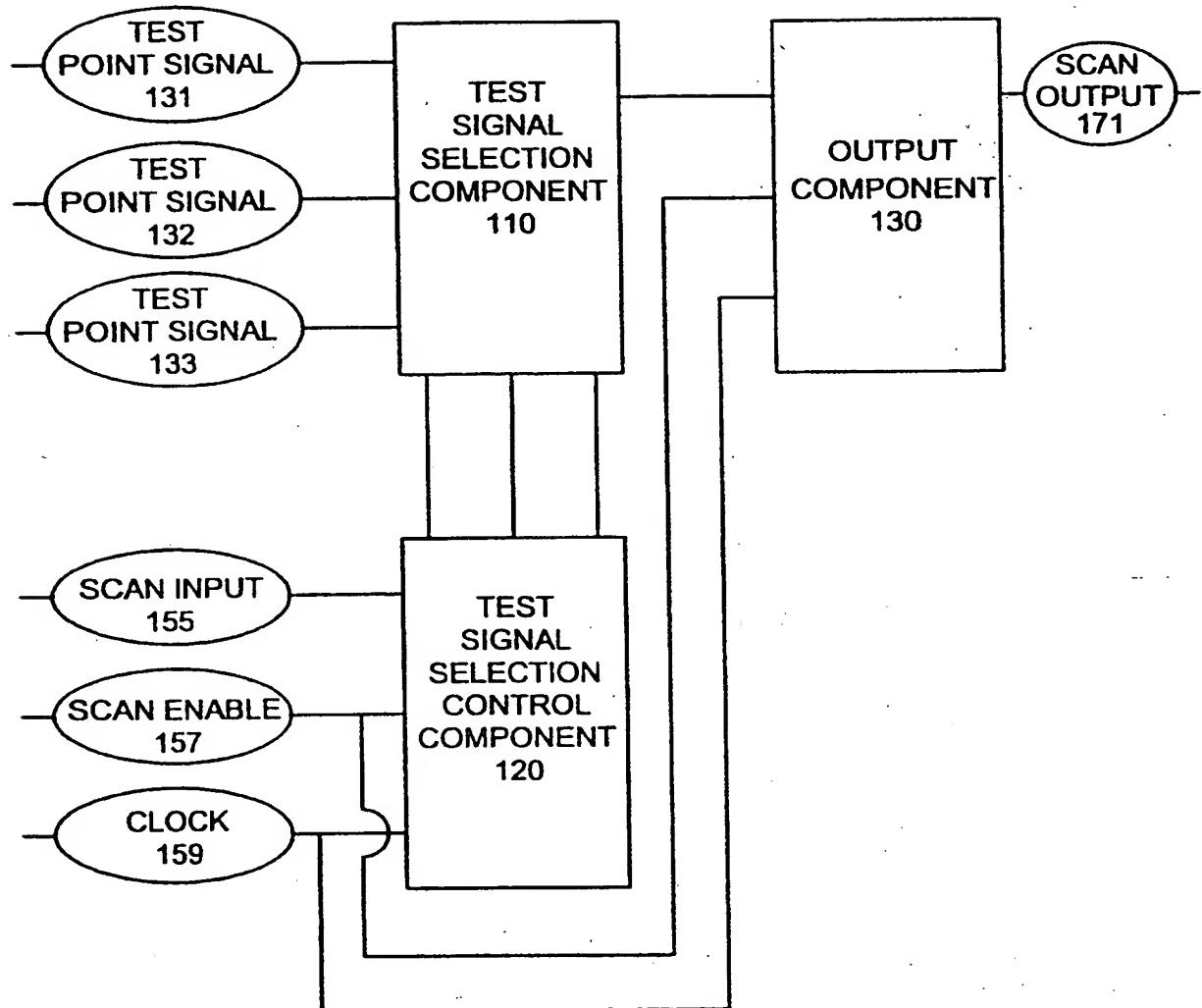


FIG.1
SUBSTITUTE SHEET (RULE 26)

200

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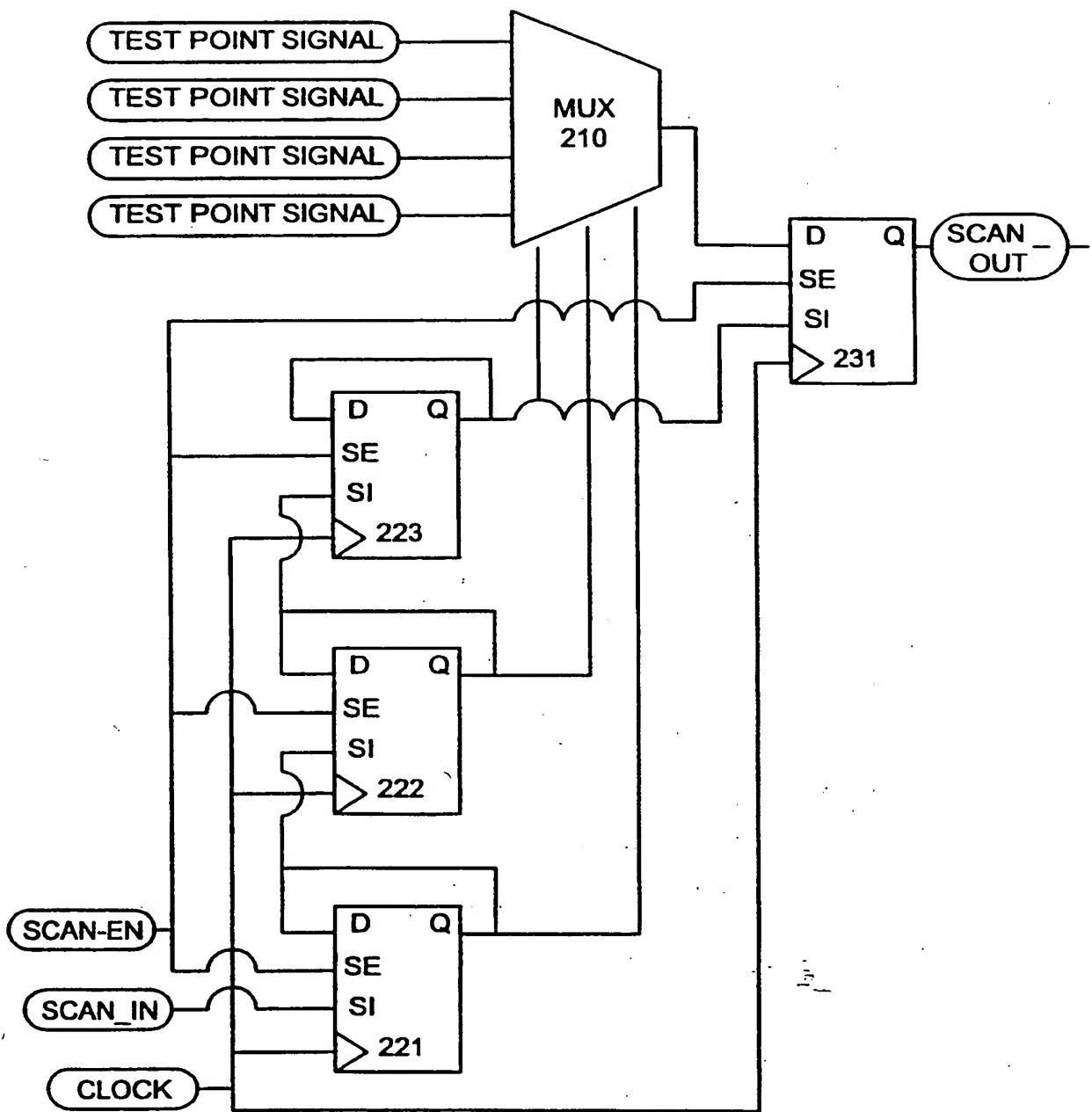


FIG.2

SUBSTITUTE SHEET (RULE 26)

300

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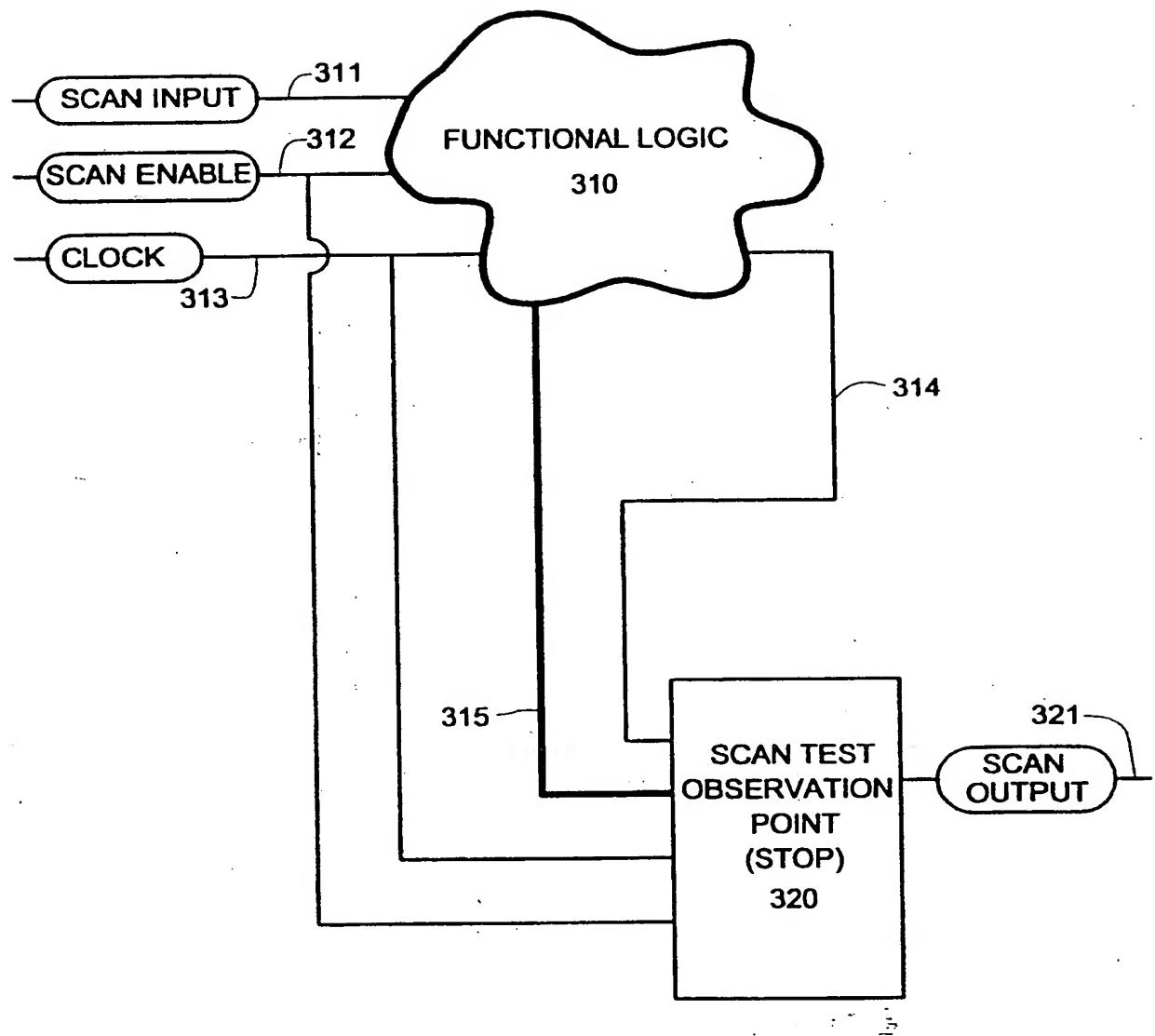


FIG.3
SUBSTITUTE SHEET (RULE 26)

400

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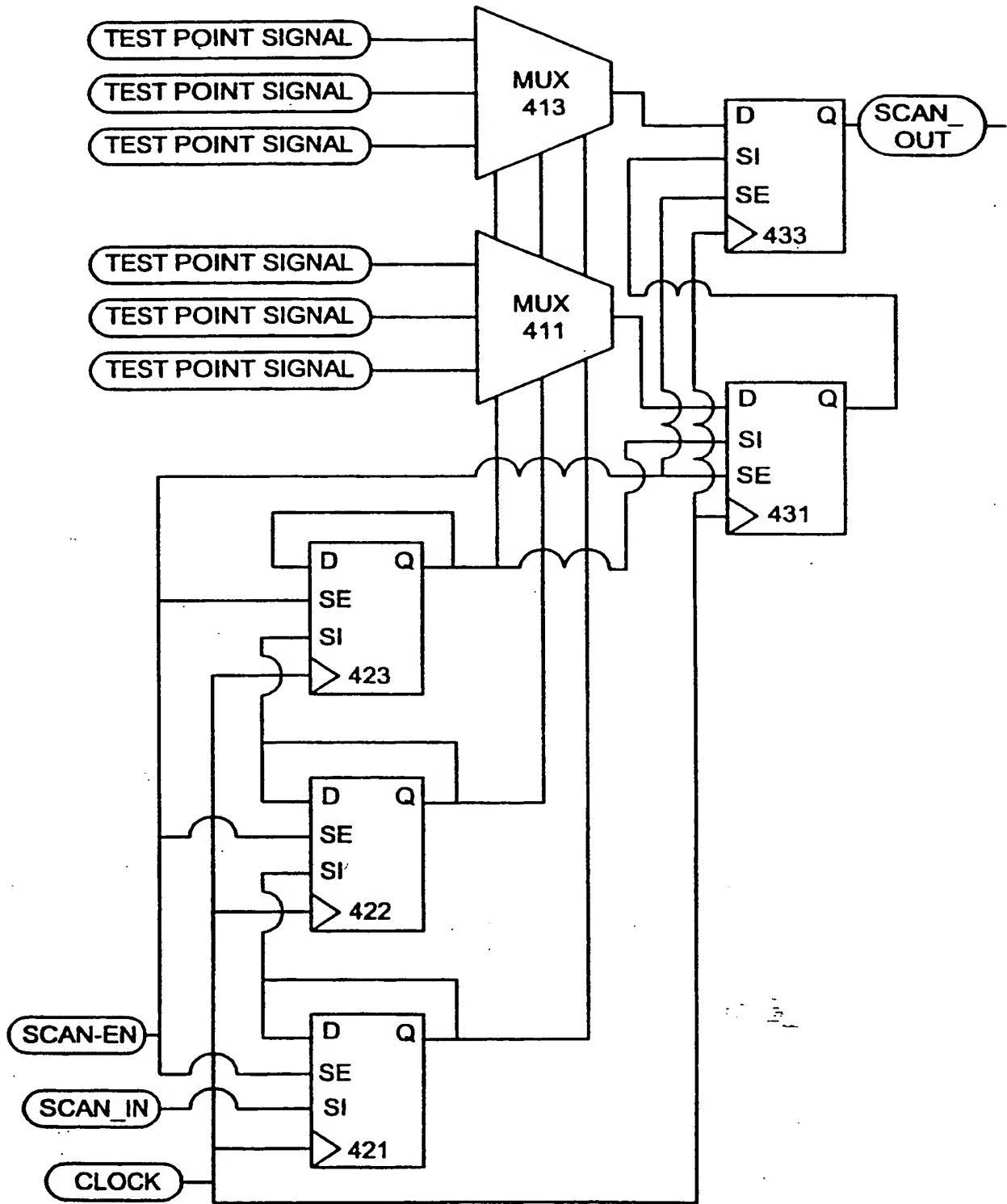
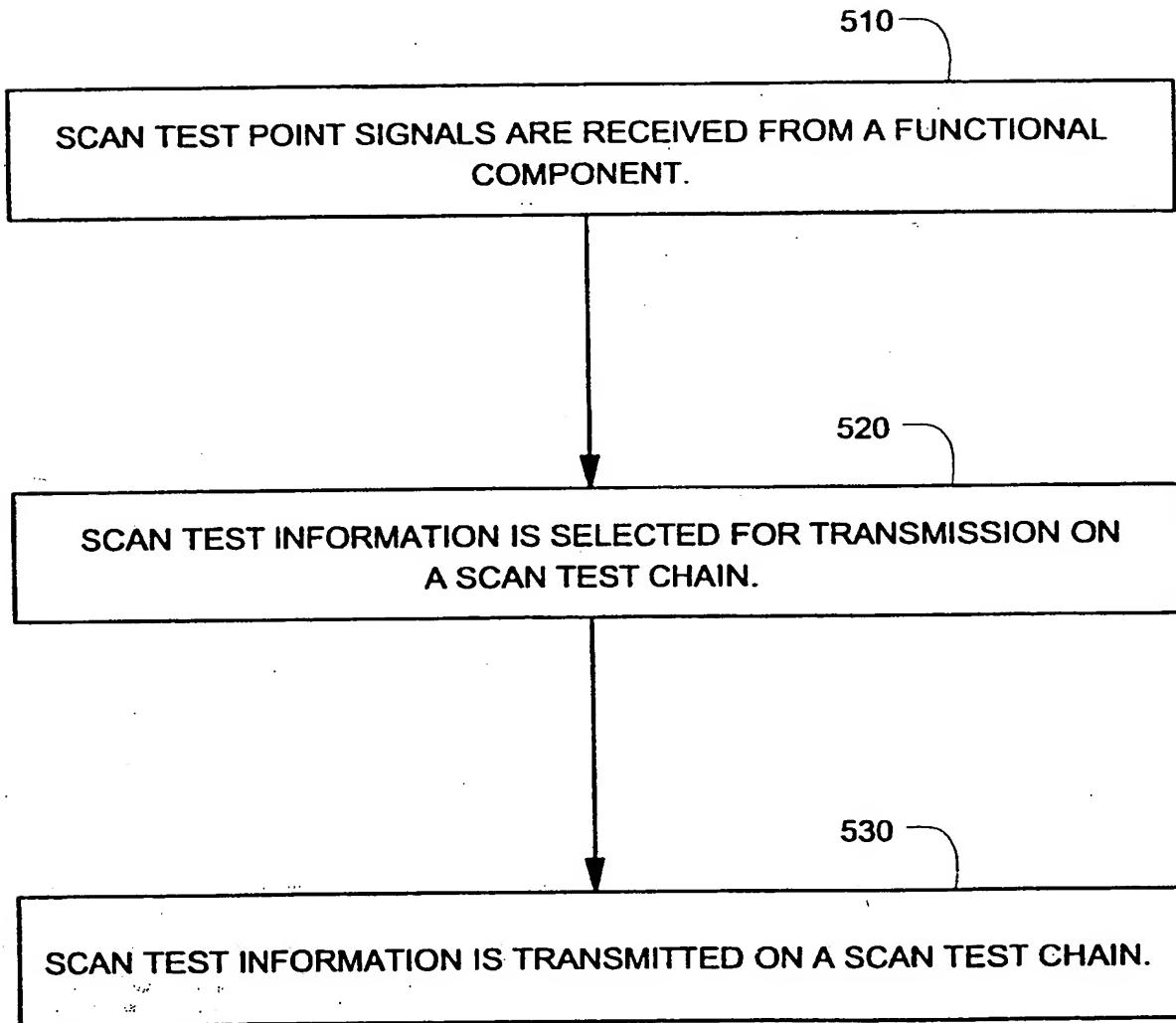


FIG.4

SUBSTITUTE SHEET (RULE 26)

500

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**FIG.5****SUBSTITUTE SHEET (RULE 26)**

INTERNATIONAL SEARCH REPORT

Inte lational Application No
PCT/US 00/27310

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G01R31/3185

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data, INSPEC, COMPENDEX, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 757 818 A (ASHURI RONI) 26 May 1998 (1998-05-26) column 1, line 39 - line 48 column 2, line 66 -column 3, line 65 abstract; figures 2,3 ---	1-3, 18-20,24
X	US 5 774 475 A (QURESHI FAZAL UR REHMAN) 30 June 1998 (1998-06-30) column 3, line 8 -column 5, line 14 abstract; figure 3 ---	1,2,5-9, 13-24 -/-

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/27310

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MAIERHOFER J ET AL: "DER JTAG BOUNDARY-SCAN" ELEKTRONIK, DE, FRANZIS VERLAG GMBH. MUNCHEN, vol. 38, no. 9, 28 April 1989 (1989-04-28), pages 108-110, 112-113, XP000037010 ISSN: 0013-5658	1,18-24
A	page 109, left-hand column, paragraph 2 -page 113, left-hand column, paragraph 2 figures 2,3,5 -----	2-17

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 00/27310

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US 5757818 A	26-05-1998	NONE		
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